



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,781	04/16/2004	George Chien	MP0347	9068
26200	7590	03/13/2006	EXAMINER	
FISH & RICHARDSON P.C.			CHOE, HENRY	
P.O BOX 1022			ART UNIT	
MINNEAPOLIS, MN 55440-1022			PAPER NUMBER	

2817

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

RD

<b>Office Action Summary</b>	Application No. 10/825,781	Applicant(s) CHIEN ET AL.	
	Examiner Henry K. Choe	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 December 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 6, 9, 14, 17, 22, 25, 30, 33 and 38 is/are rejected.
- 7) ☒ Claim(s) 2-5, 7, 8, 10-13, 15, 16, 18-21, 23, 24, 26-29, 31, 32, 34-37, 39 and 40 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

Claim 18 is objected to because of the following informalities: In lines 2-3 of claim 18, should "receive the output signal of the output signal" be --receive the output signal--?. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 6, 9, 14, 17, 22, 25, 30, 33 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh (Fig. 3) in view of Casper (Fig. 1).

Regarding claims 1, 9 and 33, Itoh (Fig. 3) discloses an amplifier circuit comprising an amplifier (66, 68) operable to receive an input signal (26, 28) and a feedback signal (a connection between an emitter of transistor 16 and an inverting input of 66, a connection between an emitter of transistor 18 and an inverting input of 68) and produce an intermediate signal (output of 66, output of 68), and a differential circuit (16, 18, R1, 30, 32, 20, 22) which is operable to receive the intermediate signal (output of 66, output of 68) and produce an output signal (a signal coming out of the output terminal 20, a signal coming out of the output terminal 22) and the feedback signal (a connection between an emitter of transistor 16 and an inverting input of 66, a connection between an emitter of transistor 18 and an inverting input of 68). As described above, Itoh (Fig. 3) discloses all the limitations in the claims except for that the differential circuit being a variable offset circuit. Casper (Fig. 1) discloses an amplifier circuit comprising a variable offset circuit [(114, 116); see column 2, lines 2-15]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known variable offset circuit such as a variable current source in place of the fix current source of the Itoh (Fig. 3), such as

Art Unit: 2817

taught by Casper (Fig. 1) in order to provide the advantageous benefit of cancelling the offset voltage (see column 2, lines 9-15).

Regarding claims 6, 14, 22, 30 and 38, Itoh (Fig. 3) discloses an amplifier circuit comprising an amplifier (66, 68) operable to receive an input signal (26, 28) and a feedback signal (a connection between an emitter of transistor 16 and an inverting input of 66, a connection between an emitter of transistor 18 and an inverting input of 68) and produce an intermediate signal (output of 66, output of 68), and a differential circuit (16, 18, R1, 30, 32, 20, 22) which is operable to receive the intermediate signal (output of 66, output of 68) and produce an output signal (a signal coming out of the output terminal 20, a signal coming out of the output terminal 22) and the feedback signal (a connection between an emitter of transistor 16 and an inverting input of 66, a connection between an emitter of transistor 18 and an inverting input of 68). As described above, Itoh (Fig. 3) discloses all the limitations in the claims except for that the differential circuit being a variable gain amplifier circuit. Casper (Fig. 1) discloses an amplifier circuit comprising a variable gain amplifier circuit [(102, 104, 106, 108, 114, 116, 110, 112); see column 3, lines 1-48]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known variable gain amplifier circuit in place of the differential circuit of the Itoh (Fig. 3), such as taught by Casper (Fig. 1) in order to provide the advantageous benefit of controlling the gain of the amplifier circuit (see column 3, lines 1-48).

Claims 17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasperkovitz (Fig. 2) in view of Itoh (Fig. 3) and Casper (Fig. 1).

Kasperkovitz (Fig. 2) discloses a receiver (Fig. 2) which is operable to receive a modulated carrier signal (see lines 1-3 of abstract) and having an amplifier (RA1-RAn). However, Kasperkovitz (Fig. 2) does not disclose the internal structures of the amplifier (RA1-RAn). Itoh (Fig. 3) discloses an amplifier circuit comprising an amplifier (66, 68) operable to receive an input signal (26, 28) and a feedback signal (a connection between an emitter of transistor 16 and an inverting input of 66, a connection between an emitter of transistor 18 and an inverting input of 68) and produce an intermediate signal (output of 66, output of 68), and a differential circuit (16, 18, R1, 30, 32, 20, 22) which is operable to receive the intermediate signal (output of 66, output of 68) and produce an output signal (a signal coming out of the output terminal 20, a signal coming

Art Unit: 2817

out of the output terminal 22) and the feedback signal (a connection between an emitter of transistor 16 and an inverting input of 66, a connection between an emitter of transistor 18 and an inverting input of 68). As described above, Kasperkovitz (Fig. 2) and Itoh (Fig. 3) discloses all the limitations in the claims except for that the differential circuit being a variable offset circuit. Casper (Fig. 1) discloses an amplifier circuit comprising a variable offset circuit [(114, 116); see column 2, lines 2-15]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known variable offset circuit such as a variable current source in place of the fix current source of the Itoh (Fig. 3), such as taught by Casper (Fig. 1) in order to provide the advantageous benefit of cancelling the offset voltage (see column 2, lines 9-15 of Casper). Furthermore, It would have been obvious to substitute the combination of Itoh (Fig. 3) and Casper (Fig. 1) amplifiers in place of Kasperkovitz's amplifier (RA1 to RAn of Kasperkovitz) since Kasperkovitz discloses a generic amplifier thereby suggesting that any equivalent amplifier would have been usable in Kasperkovitz's reference including the combination of Itoh (Fig. 3) and Casper (Fig. 1).

### ***Allowable Subject Matter***

Claims 2-5, 7, 8, 10-13, 15, 16, 18-21, 23, 24, 26-29, 31, 32, 34-37, 39 and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

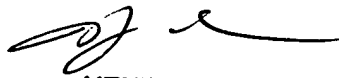
Art Unit: 2817

***Reasons for Allowance***

The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 2, 10, 18, 26 and 34, the closest prior art of record, Itoh (Fig. 3) does not disclose the following limitations: a correction circuit which is operable to receive the output signal. Regarding claims 7, 15, 23, 31 and 39, the closest prior art of record, Itoh (Fig. 3) does not disclose the following limitations: the amplifier is a unity gain buffer amplifier. Regarding claims 8, 16, 24, 32 and 40, the closest prior art of record, Itoh (Fig. 3) does not disclose the following limitations: the circuit is compliant with one or more of the Institute of Electrical and Electronics Engineers standards.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

  
**HENRY CHOE**  
**PRIMARY EXAMINER**

#1100